(a) In supporting his rejections, Examiner asserts that the means provided-for in the claims of Nilssen's patents "provide the waveforms presently claimed".

That assertion, which is presented by Examiner entirely without evidence or explanation, is erroneous.

For instance, present claim 27 includes a feature whereby "the absolute magnitude of the DC voltage is substantially higher than the peak absolute magnitude of the power line voltage. This feature is not in any manner whatsoever suggested by any of the claims in Nilssen's patents.

For another instance, present claim 28 includes "an inductor and a capacitor ... resonant at ... the fundamental frequency of the ... inverter voltage"; which feature is not in any manner suggested by any of the claims of Nilssen's patents.

For still other instances, claims 29 and 30 --- etc.

(b) Then, Examiner goes on to state that:

"One of ordinary skill ... would have found the presently claimed waveform generating means obvious in view of the means claimed in the patents which generate the waveforms."

This statement by Examiner is incomprehensible to Applicant.

In any case, Applicant's claims deal with much more than means to generate voltages of certain waveforms.

Examiner rejected claims 13-15 and 25-30 under 35 USC 102b as being anticipated by Nomura et al. ("Nomura") or Schreiner.

Applicant traverses these rejections for the following reasons.

(c) Exemplary claim 13 includes:

"... inverter means having a first periodically conducting transistor operative to conduct in its forward direction only during a first conduction period; the first conduction period having a duration shorter than half the duration of the fundamental period".

This feature is not disclosed by either Nomura or Schreiner.

If Examiner were to persist in his position to the contrary, he is requested to show exactly where and/or how Nomura or Schreiner describes that feature.

In this connection, Applicant informs Examiner of the fact that an ordinary bi-polar transistor is operative to conduct in its forward direction for a substantial period of time after the forward voltage bias on its base has been removed. This fact, which is well known by persons having ordinary skill in the art pertinent hereto, underlies the common practice of removing the drive voltage from the transistor base some time prior to the point at which the collector current should stop flowing; which common practice is evidenced by waveform A of Nomura's Fig. 2 and by lines 46-49 of Schreiner's column 4.

(d) Claim 27 includes a feature whereby:

"the absolute magnitude of the DC voltage is substantially higher than the peak absolute magnitude of the power line voltage".

This feature is not disclosed by either Nomura or Schreiner.

If Examiner were to persist in his position to the contrary, he is requested to show exactly where and/or how Nomura or Schreiner describes that feature.

(e) Claim 28 comprises an inverter that includes:

"an inductor and a capacitor ... resonant at or near the fundamental frequency of the alternating inverter voltage".

This feature is not disclosed by either Nomura or Schreiner.

If Examiner were to persist in his position to the contrary, he is requested to show exactly where and/or how Nomura or Schreiner describes that feature.

(f) Claim 29 comprises an inverter that includes:

"means for controlling the frequency of the alternating inverter voltage".

This feature is not disclosed by either Nomura or Schreiner.

If Examiner were to persist in his position to the contrary, he is requested to show exactly where and/or how Nomura or Schreiner describes that feature.

(g) Claim 30 comprises an inverter characterized by:

"including: (i) a periodically conducting transistor having control input terminals; and (ii) a control signal source providing an alternating control signal to the control input terminals, the peak-to-peak magnitude of the control signal being

substantially larger than twice the forward voltage drop of an ordinary semiconductor junction".

This feature is not disclosed by either Nomura or Schreiner.

If Examiner were to persist in his position to the contrary, he is requested to show exactly where and/or how Nomura or Schreiner describes that feature.

Finally, Examiner rejected claims 13-15 and 25-30 under 35 USC 103 as being unpatentable over Nomura or Schreiner.

Applicant traverses these rejections for the following reasons.

(h) Exemplary claim 13 includes:

"... inverter means having a first periodically conducting transistor operative to conduct in its forward direction only during a first conduction period; the first conduction period having a duration shorter than half the duration of the fundamental period".

This feature is neither disclosed nor suggested by either of the applied references.

If Examiner were to persist in his position to the contrary, he is requested to show exactly where and/or how Nomura or Schreiner suggests such a feature.

In this connection, Applicant informs Examiner of the fact that an ordinary bi-polar transistor is operative to conduct in its forward direction for a substantial period of time after the forward voltage bias on its base has been removed. This fact, which is well known by persons having ordinary skill in the art pertinent hereto, underlies the common practice of removing the drive voltage from the transistor base some time prior to the point at which the collector current should stop flowing; which common practice is evidenced by waveform A of Nomura's Fig. 2 and by lines 46-49 of Schreiner's column 4.

(i) Claim 27 includes a feature whereby:

"the absolute magnitude of the DC voltage is substantially higher than the peak absolute magnitude of the power line voltage".

This feature is neither disclosed nor suggested by either of the applied references.

If Examiner were to persist in his position to the contrary, he is requested to show exactly where and/or how Nomura or Schreiner suggests such a feature.

(j) Claim 28 comprises an inverter that includes:

"an inductor and a capacitor ... resonant at or near the fundamental frequency of the alternating inverter voltage".

This feature is neither disclosed nor suggested by either of the applied references.

If Examiner were to persist in his position to the contrary, he is requested to show exactly where and/or how Nomura or Schreiner suggests such a feature.

(k) Claim 29 comprises an inverter that includes:

"means for controlling the frequency of the alternating inverter voltage".

This feature is neither disclosed nor suggested by either of the applied references.

If Examiner were to persist in his position to the contrary, he is requested to show exactly where and/or how Nomura or Schreiner suggests such a feature.

(l) Claim 30 comprises an inverter characterized by:

"including: (i) a periodically conducting transistor having control input terminals; and (ii) a control signal source providing an alternating control signal to the control input terminals, the peak-to-peak magnitude of the control signal being substantially larger than twice the forward voltage drop of an ordinary semiconductor junction".

This feature is neither disclosed nor suggested by either of the applied references.

If Examiner were to persist in his position to the contrary, he is requested to show exactly where and/or how Nomura or Schreiner suggests such a feature.

CONCLUDING REMARKS

New claims 31-33 are merely independent versions of claims 27, 29 and 30, respectively.

New claim 34 recites the feature illustrated by Applicant's Figs. 3C and 3A. That is, claim 34 enunciates the fact that the inverter's switching transistor does not conduct current during the period when the instantaneous magnitude of the inverter's output voltage is in the process of changing between the first constant level to the second constant level (e.g., the period marked II in Fig. 3A).

RE-AMENDED CLAIMS in Serial No. 07/717,860

Claims 1-12 are cancelled.

13. An arrangement comprising:

a source operative to provide a DC voltage at a pair of DC terminals;

inverter means connected with the DC terminals and operative to provide an inverter voltage at a pair of inverter terminals; the inverter voltage having a fundamental period; the inverter means having a first periodically conducting transistor operative to conduct in its forward direction only during a first conduction period; the first conduction period having a duration substantially shorter than half the duration of the fundamental period; and

load means connected with the inverter terminals and operative to draw a load current therefrom; the load means including energy-storing inductor means and a gas discharge lamp.

2 ~~14.~~ The arrangement of claim ~~13~~ 1 wherein the inverter means has a second alternatingly conducting transistor operative to conduct in its forward direction only during a second conduction period; the second conduction period having a duration substantially shorter than half the duration of the fundamental period.

3 ~~15.~~ The arrangement of claim ~~13~~ 1 wherein the first conduction period has a duration shorter than one quarter of the duration of the fundamental period.

Claims 16-24 are cancelled.

4 ~~25.~~ An electronic ballast for a gas discharge lamp, comprising:

a source operative to provide a power line voltage at a set of power line terminals;

rectifier means connected with the power line terminals and operative to provide a DC voltage at a set of DC terminals; and

inverter means connected with the DC terminals and operative to provide an alternating inverter voltage at a pair of inverter terminals; the alternating inverter voltage having a fundamental period and an instantaneous magnitude that (i) during a first period, remains substantially constant at a negative level, (ii) during a second period, increases at a

substantially constant rate, (iii) during a third period, remains substantially constant at a positive level, and (iv) during a fourth period, decreases at a substantially constant rate; the sum of the durations of the four periods being equal to the duration of the fundamental period; the duration of the first period being approximately equal to that of the third period; the duration of the first period being distinctly shorter than half the duration of the fundamental period.

5 4
~~26~~. The electronic ballast of claim ~~25~~ wherein the duration of the second period is about equal to, or longer than, one tenth the duration of the first period.

6 4
~~27~~. The electronic ballast of claim ~~25~~ wherein the absolute magnitude of the DC voltage is substantially higher than the peak absolute magnitude of the power line voltage.

7 4
~~28~~. The electronic ballast of claim ~~25~~ wherein the inverter is characterized by including an inductor and a capacitor connected together and being resonant at or near the fundamental frequency of the alternating inverter voltage.

8 4
~~29~~. The electronic ballast of claim ~~25~~ wherein the inverter includes means for controlling the frequency of the alternating inverter voltage.

9 4
~~30~~. The electronic ballast of claim ~~25~~ wherein the inverter is characterized by including: (i) a periodically conducting transistor having control input terminals; and (ii) a control signal source providing an alternating control signal to the control input terminals, the peak-to-peak magnitude of the control signal being substantially larger than twice the forward voltage drop of an ordinary semiconductor diode junction.

10
~~31~~. An electronic ballast for a gas discharge lamp, comprising:

1 a source operative to provide a power line voltage at a set of power line terminals;

1 rectifier means connected with the power line terminals and operative to provide a DC voltage at a set of DC terminals; the absolute magnitude of the DC voltage being substantially higher than the peak absolute magnitude of the power line voltage; and

(c) inverter means connected with the DC terminals and operative to provide an alternating inverter voltage at a pair of inverter terminals; the alternating inverter voltage having a fundamental period and an instantaneous magnitude that (i) during a first period, remains substantially constant at a negative level, (ii) during a second period, increases at a substantially constant rate, (iii) during a third period, remains substantially constant at a positive level, and (iv) during a fourth period, decreases at a substantially constant rate; the sum of the durations of the four periods being equal to the duration of the fundamental period; the duration of the first period being approximately equal to that of the third period; the duration of the first period being distinctly shorter than half the duration of the fundamental period.

11
32. An electronic ballast for a gas discharge lamp, comprising:

(a) a source operative to provide a power line voltage at a set of power line terminals;

(b) rectifier means connected with the power line terminals and operative to provide a DC voltage at a set of DC terminals; and

(c) inverter means connected with the DC terminals and operative to provide an alternating inverter voltage at a pair of inverter terminals; the alternating inverter voltage having a fundamental period and an instantaneous magnitude that (i) during a first period, remains substantially constant at a negative level, (ii) during a second period, increases at a substantially constant rate, (iii) during a third period, remains substantially constant at a positive level, and (iv) during a fourth period, decreases at a substantially constant rate; the sum of the durations of the four periods being equal to the duration of the fundamental period; the duration of the first period being approximately equal to that of the third period; the duration of the first period being distinctly shorter than half the duration of the fundamental period; the inverter means being further characterized by including means for controlling the frequency of the alternating inverter voltage.

Cont'd 32

12
33. An electronic ballast for a gas discharge lamp, comprising:

(a) a source operative to provide a power line voltage at a set of power line terminals;

rectifier means connected with the power line terminals and operative to provide a DC voltage at a set of DC terminals; and

inverter means connected with the DC terminals and operative to provide an alternating inverter voltage at a pair of inverter terminals; the alternating inverter voltage having a fundamental period and an instantaneous magnitude that (i) during a first period, remains substantially constant at a negative level, (ii) during a second period, increases at a substantially constant rate, (iii) during a third period, remains substantially constant at a positive level, and (iv) during a fourth period, decreases at a substantially constant rate; the sum of the durations of the four periods being equal to the duration of the fundamental period; the duration of the first period being approximately equal to that of the third period; the duration of the first period being distinctly shorter than half the duration of the fundamental period; the inverter means being further characterized by including: (i) a periodically conducting transistor having control input terminals; and (ii) a control signal source providing an alternating control signal to the control input terminals, the peak-to-peak magnitude of the control signal being substantially larger than twice the forward voltage drop of an ordinary semiconductor diode junction.

13

34. An arrangement comprising:

a source operative to provide a DC voltage at a pair of DC terminals;

an inverter connected with the DC terminals and operative to provide an alternating inverter voltage at a pair of inverter terminals; the inverter voltage having a fundamental period characterized by including: (i) a first relatively long period during which the instantaneous magnitude of the inverter voltage remains at a first substantially constant level, (ii) a first relatively short period during which the instantaneous magnitude of the inverter voltage gradually changes between the first substantially constant level and a second substantially constant level, (iii) a second relatively long period during which the instantaneous magnitude of the inverter voltage remains at the second substantially constant level, and (iv) a second relatively short period during which the instantaneous magnitude of the inverter voltage gradually changes between the second and the first substantially constant levels; the duration of the first relatively long period being substantially equal to

that of the second relatively long period; the duration of the first relatively short period being substantially shorter than the duration of the first relatively long period; the inverter being characterized by including a first periodically conducting transistor conducting current in its forward direction for a substantial part of the first relatively long period, but not during any substantial part of the first relatively short period, nor during the second relatively short period; and

(b) a load connected with the inverter terminals and operative to draw a load current therefrom; the load including an energy-storing inductor and a gas discharge lamp.

Cont'd 2

19 13

~~35~~. The arrangemnt of claim ~~34~~ wherein the transistor: (i) has an emitter and a collector; and (ii) when it indeed conducts current in its forward direction, it conducts current directly between its emitter and collector without causing any substantial voltage drop thereacross.

end